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REPORT DOCUMENTATION PAGE

Form Approved OMB NO. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	Dec. 12, 1996	Final Report 5/1/93 - 8/31/96

4. TITLE AND SUBTITLE
Study of Graded Channels in MODFETS on InP Substrates

5. FUNDING NUMBERS
DAAH04-93-G-0204

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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U.S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
ARO 31180.1-EL

11. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

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14. SUBJECT TERMS	15. NUMBER IF PAGES 25
	16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Study of Graded Channel in MODFETs on InP Substrates

FINAL REPORT

Glenn Martin, Lester Eastman

U.S. ARMY RESEARCH OFFICE

Grant # : DAAH04-93-G-0204

AMXRO-ICA-L

subject : 31180-EL

Cornell University

From May 1, 1993 Through April 30,1996
extended to Aug. 30,1996

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Study of Graded Channel in MODFETs on InP Substrates

1. Foreword

This proposal was for a three-year study to optimize the quantum well channel in MODFETs on InP substrates. The work was initially based on some remarkable results that were achieved at Cornell University for the industry standard PHEMT (AlGaAs/InGaAs/GaAs) structure. This work showed that the electron sheet density and consequently the channel current could be increased substantially by linear grading the Indium composition in the $In_xGa_{1-x}As$ channel and by modulation doping on both sides of the channel (double-doping). The major improvements that were shown with the graded channel double-doped MODFETs on GaAs were in the carrier mobility and consequently the output current. An additional benefit of the work was in reduced gate leakage currents and increased drain-source breakdown voltages, due to reduced electric fields in the 2DEG.

The goal of this contract was to apply the successful design techniques used on the GaAs PHEMTs to the relatively immature AlInAs/InGaAs MODFET structure on InP. AlInAs/InGaAs MODFETs on InP substrates typically have yielded the highest frequency response and the lowest noise figures. However, the low breakdown voltage in such InP-based MODFETs seriously limits the power level that these devices have. The reduced gate leakage that resulted from the linear graded channels on the GaAs PHEMTs was expected to substainly improve the breakdown voltages for the InP-based MODFETs.

Results from this contract was a successful demonstration for the first time of InP-based MODFETs operating above 125°C with minimal DC and RF degradation with record two dimensional electron sheet densities ($>8.0 \times 10^{12} cm^{-2}$). The MODFET structure was double-doped and double-strained with a parabolically graded channel. To achieve this final result we performed fundamental experiments during the duration of the grant to study the spacer layer thickness, Schottky barrier enhancements and stress compensation schemes.

2A. Statement of the problem studied

MODFETs on InP substrates have yielded the highest frequency response and the lowest noise figure, both due mostly to the 30% higher electron average transit velocity in the lattice-matached $In_{.53}Ga_{.47}As$ channel, compared to the 1.8 - 2.0×10^7 (cm/s) velocity for electrons in optimized channels on GaAs substrates. However, the low breakdown voltage in such InP-based MODFETs seriously limits the power level that these devices have.

In a study [1,3] using psuedomorphic $In_yGa_{1-y}As$ channels on GaAs substrates, some remarkable results have been achieved. By doping both sides of the channel, and by grading the Indium composition in the channel, electron sheet density has been increased to 4×10^{12} cm^{-2}, yielding 800 mA/mm channel current. In addition, the source-drain breakdown voltage at low current has been raised from 4 V to 7 V. In most MODFETs, this breakdown voltage drops substainially as the channel current is raised 25-30 % of full channel current. Above this current the breakdown voltage can rise moderately for GaAs-based devices, but continues to fall, more slowly, as current is raised for InP-based devices. Additionally there is a serious gate leakage current under moderate forward gate bias, even for GaAs-based MODFET's.

The two-dimensional electron gas (2DEG) is thin in all previous structures, and is crowded against the quantum well heterojunction. There are two, distinct, such 2DEGs when doping is placed above and below the channel. In this latter case, the potential in the middle of the quantum well is high, due to the space charge effects of the 2DEGs, one on each side. The ground state in the quantum well is actually broken by the bending of the conduction band (charge accumulation). The total electron distribution in the quantum well is a superposition of two triangular wells (one from each side) which creates the two distinct peaks in the free carrier profile. These peaks can be minimized by raising the ground state above the peak of the band bending in the conduction band. One way to do this is by increasing the Indium fraction in the center, compared to the Indium fraction at the sides [1] which minimizes the band bending in the quantum well.

A computer program has been developed and used at Cornell [2], incorporating both Schrodinger and Poisson equations, to yield the electron spatial distribution for any Indium fraction profile. This program, called "C-band" has been used to predict the benfits of grading Indium in the conduction channel of pseudomorphic MODFETs on GaAs substrates. Experiments have been carried out with Indium rising linearly from 15 % to 22 % and falling back linearly to 15 %. With double doping, such a channel allowed 4×10^{12} cm^{-2} electron sheet density with a mobility of 7,230 $cm^2(Vs)^{-1}$. When 0.3 μm MODFET's were made [3] with this graded-channel material, the maximum channel current was 800 mA/mm, which is 15 % higher, and the breakdown voltage was 75 % higher, than was the case for a uniform channel with 20 % Indium composition. Also, under 1 V forward bias, the gate leakage current in the graded-channel devices is nearly zero for all drain-source voltage values, while it is ~ 30 mA/mm for the double-doped channels with constant Indium fraction[3]. The low-field mobility was also 10 % higher in the graded channel at room temperature [3].

It is clear why the electron sheet density is high in such channels with

increased Indium fraction in the center of the quantum well. The electron density is more uniformly distributed across the entire channel, rather than having two sharp peaks near the two hererojunctions (caused by a break in the ground state). This is due to the lowering of the conduction band in the middle of the quantum well which results in the ground state being constant in the quantum well (occupied n = 1 states). The mobility is higher because the electrons interact less with the heterojunctions, which may not be atomically planar, and which may support interface phonons as an additional scatttering mechanism. The breakdown voltage is higher because the undepleted electron sheet density is thicker in the case of the graded Indium channel. The electric field caused by the drain-source voltage is lower, for a given voltage, because of the increased radius of curvature of the constant potential surfaces near the source end of the thicker undepleted 2DEG.

In addition to predicting the electron distribution function in such a MODFET structure, it is necessary to predict the limits on stress to prevent dislocations. Such a program has been developed at Cornell [4], originally for use in pseudomorphic multiple quantum well structures for lasers capable of high speed modulation. In the case of GaAs substrates, all of the strain has been of the two-dimensionsal compression type. For InP substrates, where $In_{.53}Ga_{.47}As$ and $In_{.52}Al_{.48}As$ are lattice matched, both two dimensional tension as well as the two-dimensional compression are possible, especially in the design of the channel. Thus the layered structure net compression or tension can be minimized. One example is the case of $In_yGa_{1-y}As$ on InP with y=.53 + y1 cos(bz) where y1 = .25 and a single period of the cosine being ~ 150 Å. It yielded an electron sheet density of $2.2 \times 10^{12} cm^{-2}$ in a single period channel, with a room mobility of 9,700 $cm^2(Vs)^{-1}$, all for single-sided doping. The double-sided doping should yield $4 \times 10^{12} cm^{-2}$ with ~ 10,000 cm2/v s mobility at room temperature.

The gate leakage, under forward bias, is reduced because the high, peaked electron density, normally obtained, has been lowered and broaded across the quantum well. This lowers the thermionically-assisted tunneling of the electrons from the channel into the gate. It is not yet certain what Indium fraction profile will be optimum. Linear symmetrical grading in 2 steps, parabolic grading, cosh or cosine grading are possibilities of interest. A modified "C-band" computer program, capable of predicting electron distributions in $In_yGa_{1-y}As$ with its different properties on InP, compared to those on GaAs, will be developed.

2B. Summary

PSeudomorphic MODFETs (SMODFET) have become the new high speed transistor for microwave applications. Basic advantage of the SMODFETs electrical performance over MESFETs and MISFETs is due to the use of quantum

wells which result in higher mobility and increased current capability. Mobility is a measure of how easily a charge carrier (electron/hole) can move. The electrical current capability of a transistor is controlled by changing the concentration of charge carriers (electron/holes) in the channel. Increasing the concentration of charge carriers above a physical limit causes a drastic decrease in mobility. This point of decreasing mobility is dependent upon the composition and materials used (height/width of the quantum well) in making the SMODFET. It has been found that by varying the indium concentration (x) in an $In_XGa_{1-X}As$ channel one can improve the electrical capability of the quantum well. This enhanced quantum well results in higher charge density and mobility, yielding a higher current capability for the SMODFET as shown in Figure 1a.

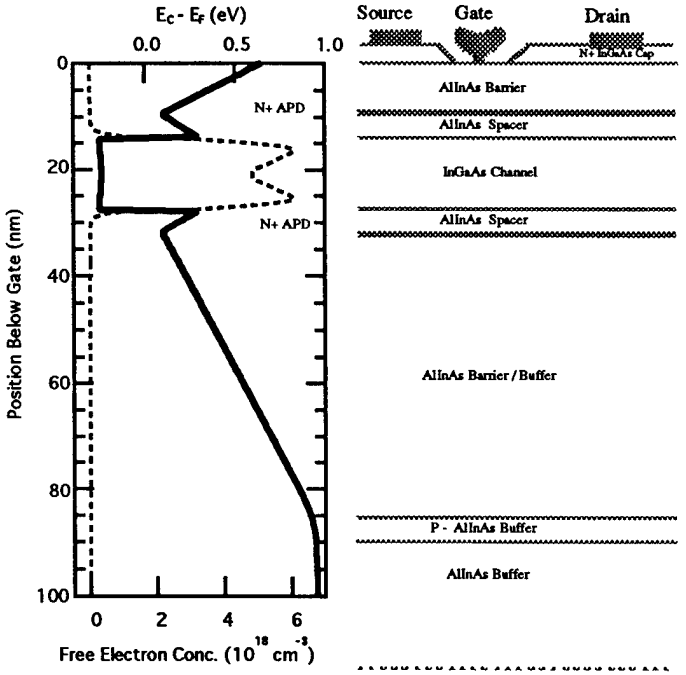


Figure 1a Conduction Band (solid) and free electrons (dashed) vs position in a double modulation doped MODFET with a parabolically graded channel and a buried p-layer in the buffer

A one-dimensional computer program which solves Schrödinger and Poisson equation simultaneously has been extended to optimize the design of MODFETs with the following features; pseudomorphic graded channels, pseudomorphic barriers, double sided doping and buried p-layers. Figure 2 show a double doped SMODFET on InP with and without a parabolically graded channel. As can be seen the separation of the energy levels in the quantum well (E1 and E2) by grading the channel will result in the higher charge density.

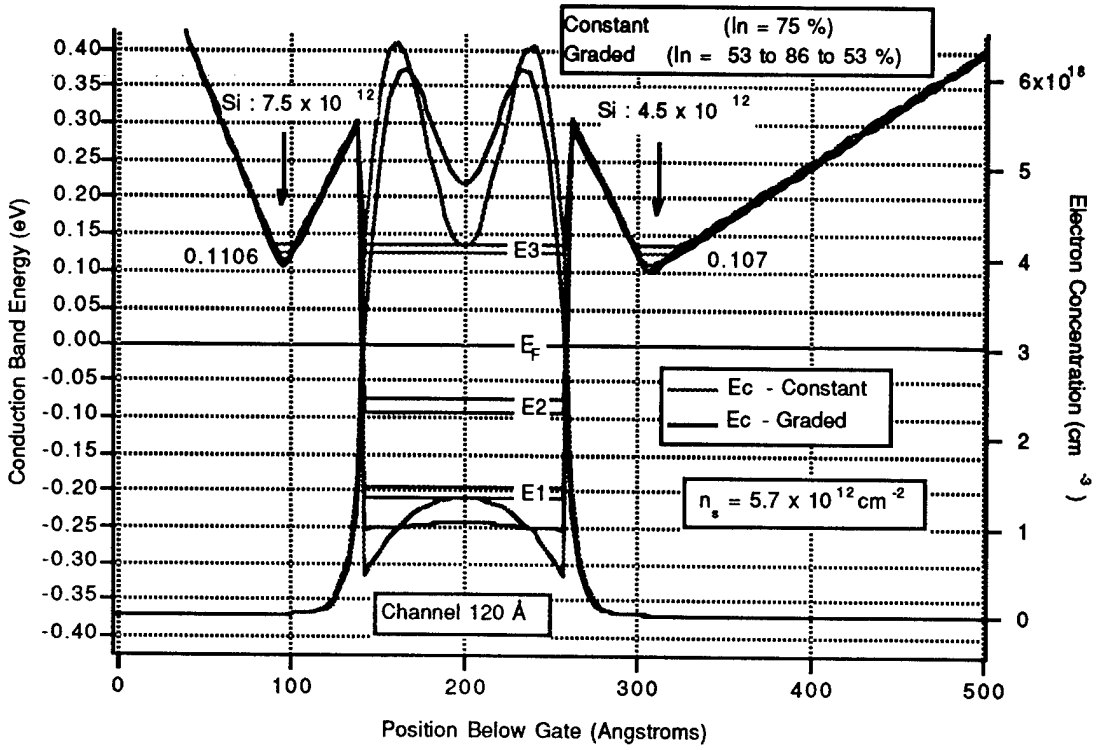


Figure 1b Double-Doped AlInAs/InGaAs Graded Channel SMODFET with uniform and a parabolically graded channel. Comparison of energy states in the channel with constant indium and parabolically graded channel on InP substrates

A simple model has been developed and used to predict and show the advantages of pseudomorphic MODFETs with graded channels [5]. The band bending in the channel caused by the charge accumulation in the full channel is easily calculated by applying Poisson's equation in the channel [8]. Integrating twice yields a simple parabolic equation (1) for the conduction band bowing.

$$\frac{\partial}{\partial z}\left(\frac{\partial}{\partial z} V\right) = -\frac{\rho}{\varepsilon} \qquad V = -\frac{\rho}{\varepsilon}\left[\frac{z^2}{2}\right] \tag{1}$$

Using equation (2) for the charge density (L_s is the channel thickness), we can calculate the maximum deflection of the conduction band in the channel for double and single-doped SMODFETs.

$$\rho_c = \frac{q n_s}{L_s} = \frac{q n_s}{2a} \tag{2}$$

Substituting equation (2) into equation (1) yields the following design equation for a single-doped MODFET (max. DV @ z=2a),

$$V_{channel} = -\frac{\rho}{\varepsilon}\left[\frac{z^2}{2}\right] = -\frac{1}{\varepsilon}\left[\frac{qn_s}{2a}\right]\left[\frac{(2a)^2}{2}\right] = -\frac{qn_s a}{\varepsilon} \qquad (3)$$

and for a double-doped MODFET (max. DV @ z=a).

$$V_{channel} = -\frac{\rho}{\varepsilon}\left[\frac{z^2}{2}\right] = -\frac{1}{\varepsilon}\left[\frac{qn_s}{2a}\right]\left[\frac{(a)^2}{2}\right] = -\frac{qn_s a}{4\varepsilon} \qquad (4)$$

Since the band bending in the channel varies as a parabola (equation 1), we can vary the indium concentration in the channel parabolically to directly cancel the voltage (flatten E_c). This parabolic variation of the indium concentration (x) assumes that DE_c is to the first order linear with x (Figure 2).

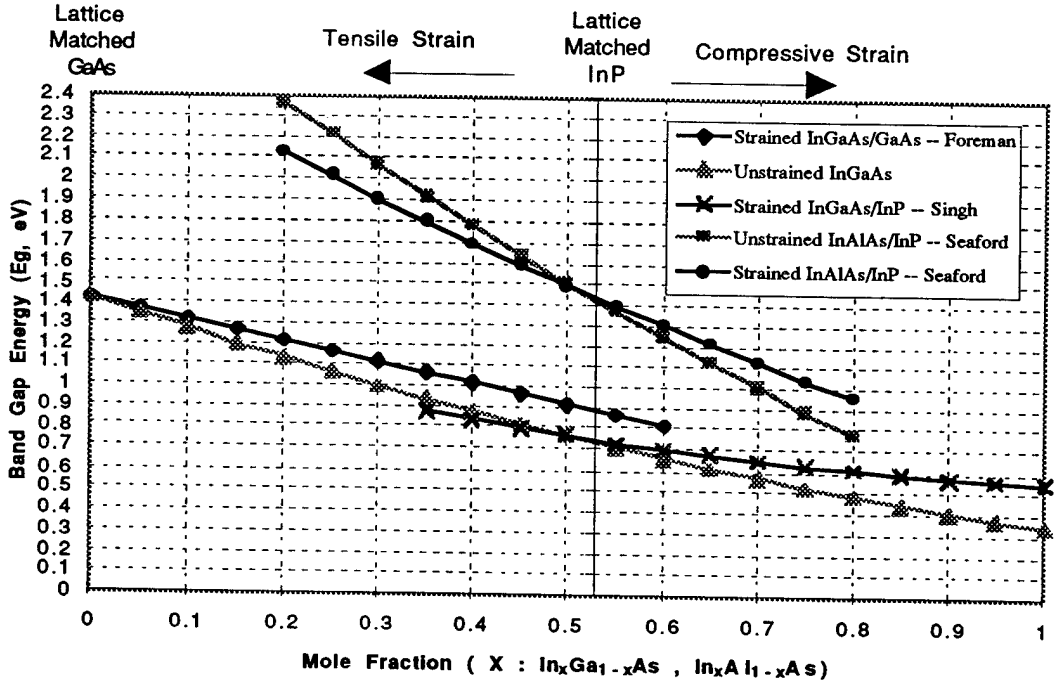


Figure 2 Band Gap Energy vs. Indium Mole Fraction for InGaAs and AlInAs ternary compounds for (bulk) and strained.

The minimum and maximum values of this parabolic grade are dependent on the voltage deflection and the strain limits of the material as calculated by the Matthews/Blakeslee (M/B) limit (equation 5) [3].

$$\frac{\Delta a}{a} = \left(\frac{a_0}{\sqrt{2}}\right)\left(\frac{1}{2\pi h_c}\right)\frac{\left(1-\frac{\vartheta}{4}\right)}{(1+\vartheta)}\left[\ln\left(\frac{h_c}{a_0/\sqrt{2}}\right)+1\right] \qquad (5)$$

Where h_c is the critical thickness, ϑ is Poisson's ratio and $\Delta a/a$ is the fractional strain. The average value of a parabola is two thirds of the maximum. Hence we figure the M/B limit for a specific channel thickness and make this the average value of the parabolic grade to stay within the strain limits. As a general rule we take 5/8 of the bandgap difference for GaAs based MODFETs and 5/7 for the InP based MODFETs for the conduction band discontinuity [9]. This conduction band discontinuity is used for the barrier height in calculating the energy levels in the channel.

The electric dipole across the spacer layer just outside the channel is derived from the simple electrostatic relation **D** = e***E** and is shown in equations (6, 7, 8) [8].

$$E = \frac{V}{x} = \frac{D}{\varepsilon} = \frac{q n_s}{\varepsilon} \qquad (6)$$

For single-doped MODFETs, and for double-doped MODFETs (assuming that the total channel charge is split equally between the top and bottom doping) with W_S being the spacer thickness.

$$\Delta V_{spacer} = \frac{q n_s}{\varepsilon} W_s, \text{ single-doped MODFET} \qquad (7)$$

$$\Delta V_{spacer} = \frac{q n_s}{2\varepsilon} W_s, \text{ double-doped MODFET} \qquad (8)$$

Assuming that the channel is small enough that the density of states is quantized in two dimensions, the calculation of the 2D density of states is given as in equation (9).

$$D = \frac{m^*}{\pi \hbar^2} \qquad (9)$$

With a graded channel (assuming a flat quantum well) the quantized energy levels (E_n) are calculated from simple quantum mechanics [10]. For a well with infinite walls the energy levels are calculated as shown in equation (10).

$$E_n = E_1 * n^2 \quad \text{with} \quad E_1 = \frac{\hbar^2 \pi^2}{2m^*(2a)^2} = \frac{\hbar^2 \pi^2}{8m^*(a)^2} \qquad (10)$$

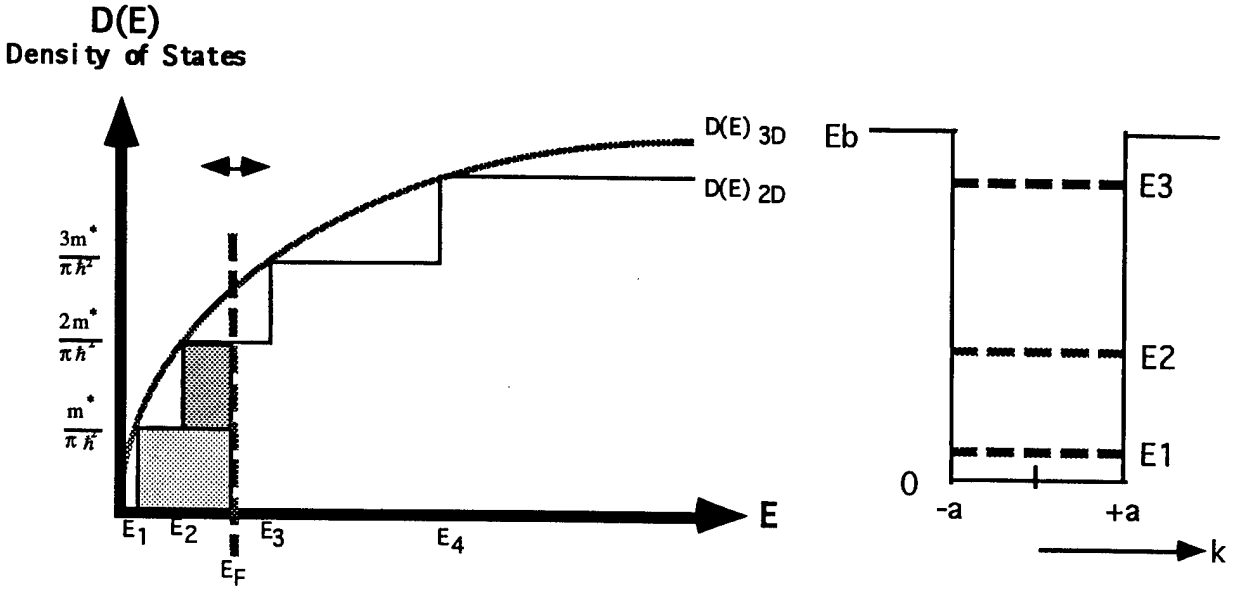


Figure 3 a) Three and two dimensional density of states versus energy for determining sheet charge (n_s) using the area rule. b) Energy levels (E_n) in a quantum well with a finite barrier (E_b).

For a quantum well with finite walls (Figure 3b) we have to solve the following transcendental equations (equation 11) with k_{en} inside the well and k_{en} outside the well. This assumes m* (carrier effective mass) is the same inside and outside the quantum well.

$$\begin{aligned} \kappa_{e1}\tan(\kappa_{e1}a) &= k_{e1} \\ -\kappa_{e2}\cot(\kappa_{e2}a) &= k_{e2} \end{aligned} \qquad (11)$$

with $\kappa_{e_n} = \frac{\sqrt{2m^*E_{e_n}}}{\hbar}$ and $k_{e_n} = \frac{\sqrt{2m^*(E_b - E_{e_n})}}{\hbar}$

E_b = barrier height

a = (channel thickness) / 2

From Figure 3a, we can calculate the sheet charge with a simple area rule as shown in equation (12)

$$n_s = \frac{m^* q}{\pi\hbar^2}\left[(E_F - E_1) + (E_F - E_2) + \cdots + (E_F - E_N)\right] \qquad (12)$$

From Figure 4, and using conservation of energy, we can calculate the fermi energy (E_F) as shown in equation (13)

$$E_F = \left[\Delta E_C - V_{prob}\right] - \frac{2}{3}V_{channel} - \Delta V_{spacer} \qquad (13)$$

with ΔE_C = conduction band discontinuity

V_{prob} = barrier probability of occupancy (0.12v for a 1% probability)

$V_{channel}$ = space charge effect potential in the channel (equation 3 or 4)

ΔV_{spacer} = voltage due to charge dipole across spacer ($E_s * W_s$)

Solving equations (12) and (13) simultaneously, yields the sheet charge(n_s) and fermi energy(E_F) for the 3D-SMODFETs.

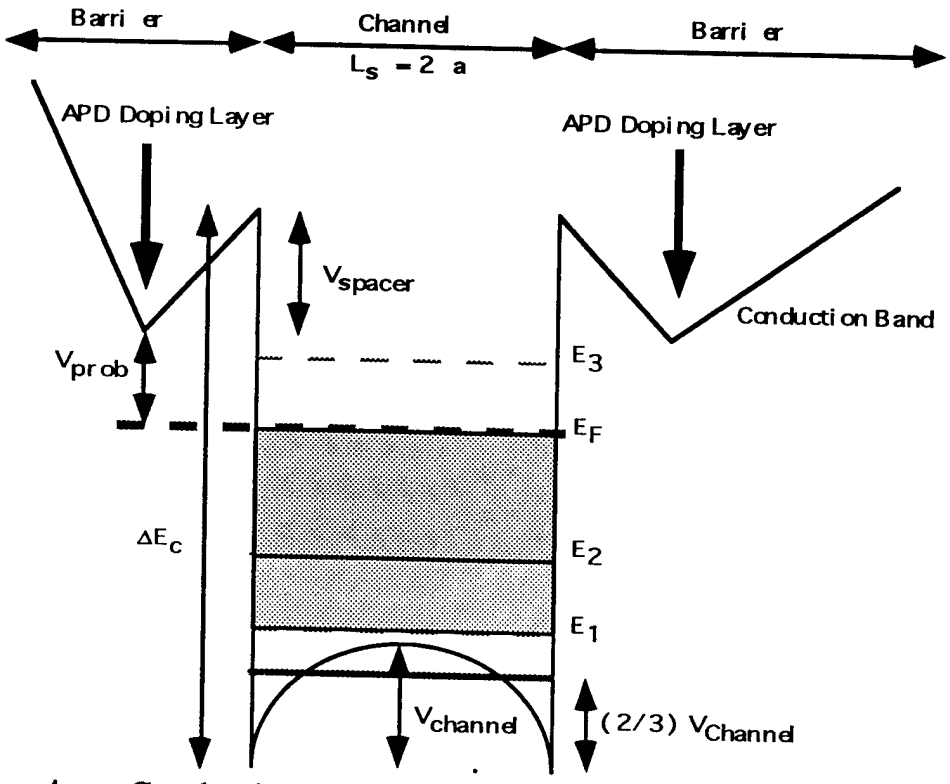


Figure 4 Conduction band versus position below gate with quantized energy levels.

The simple model that was developed and verified with this contract for the AlInAs/InGaAs MODFET on InP substrates is being continually extrended to optimize the InGaP/InGaAs MODFET on GaAs and the AlGaN/InGaN MODFET. The simple model assumes that the band bending of the conduction band can be completly canceled by the parabolic grading of the Indium in the InGaAs quantum well. With this assumption the quantized energy levels inside the quantum well can be solved from the textbook analysis of a quantum well with finite barriers. Conservation of energy (Kirchoff Voltage law) and knowing the quantized energy levels in the well allows us to write write two simultaneous equations which are easily solved for the complete solution of the MODFET [5]. By varing the channel thickness and keeping the other parameteres constant we can easily plot the 2DEG vs channel thickness for single and double modulation doped structures as shown in Figure 5a and 5b.

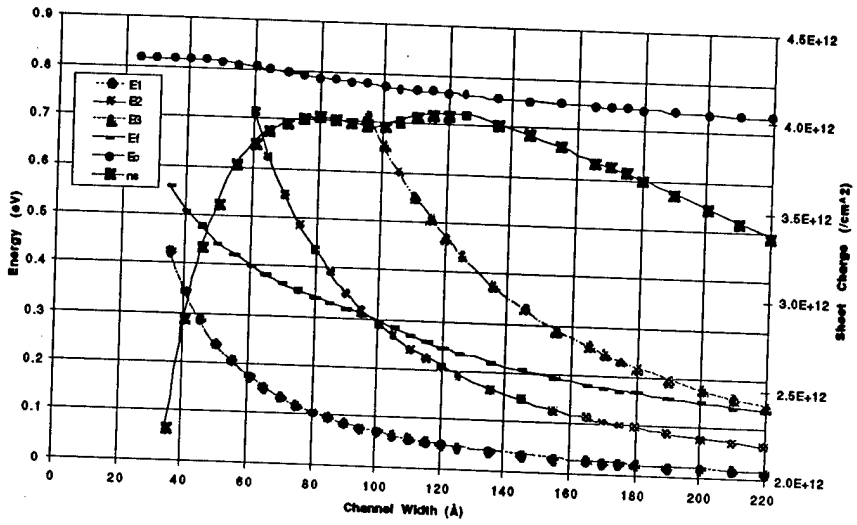


Figure 5a Single-Doped Double-Strained MODFET with $Al_{0.60}In_{0.40}As$ barriers and parabolically graded $In_XGa_{1-X}As$ channels. The average value of In (X) was calculated from the Matthews/Blakeslee critical thickness equation. The ground state (diamond), first excited state (square), second excited state (triangle), Fermi energy (bar) and the maximum sheet charge (star) are shown versus channel thickness.

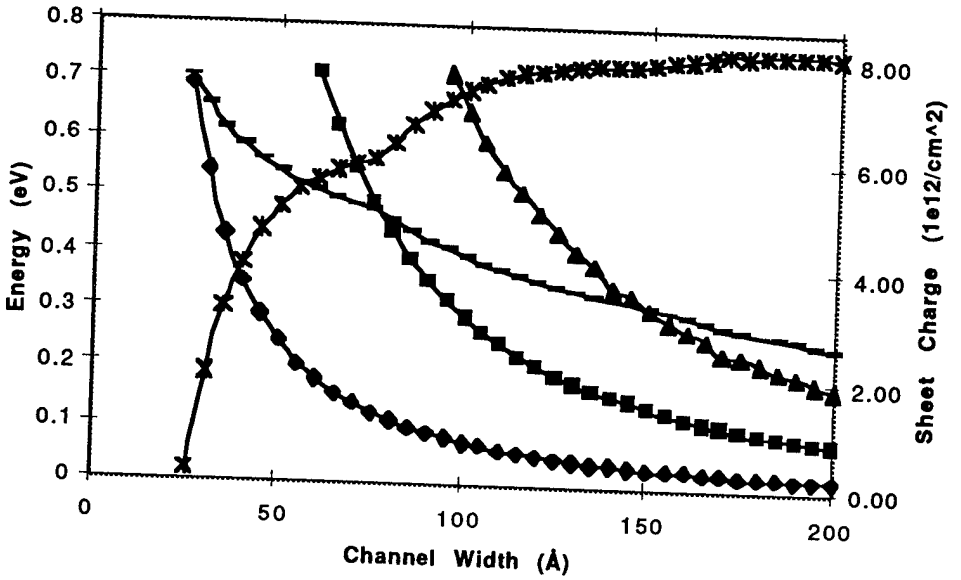


Figure 5b Double-Doped Double-Strained MODFET (3D-SMODFET) with $Al_{0.60}In_{0.40}As$ barriers and parabolically graded $In_XGa_{1-X}As$ channels. The average value of In (X) was calculated from the Matthews/Blakeslee critical thickness equation. The ground state (diamond), first excited state (square), second excited state (triangle), Fermi energy (bar) and the maximum sheet charge (star) are shown versus channel thickness.

Sets of MBE experiments in conjunction with QED were designed to optimize the growth of InP based SMODFETs with graded channels. These experiments were begun during the summer of 1994 and are still being pursued with MBE material now coming from Wright Laboratory (WPAFB). Results of many of the MBE experiments have been formally published [5,6,7,8]. A materials related problem of clustering of the binaries (AlAs, InAs and GaAs) when the lattice matched compositions were grown and processed. To solve this clustering we have grown $Al_{.6}In_{.4}As$ and $In_{.65}Ga_{.35}As$ ternaries which has minimized the clustering and allowed us to achieve a record 2DEG, current, and high temperature performance of InP-based MODFETs [7,8]. Currently the clustering of the ternaries is being agressively studyed at Wright Laboratories with cross-sectional STM (XSTM) as the main instrument for analysis.

Using molecular beam epitaxy we grew the 3D-SMODFET structure on Iron doped InP substrates. The devices were grown as follows: 2500 Å of $Al_{0.48}In_{0.52}As$ as a buffer, 200 Å of $Al_{0.6}In_{0.4}As$ as a lower barrier, lower atomic planar doping (APD) of Si, 40 Å of $Al_{0.6}In_{0.4}As$ as a spacer, 200 Å of $In_xGa_{1-x}As$ (x_{av}=.65) for the channel, 40 Å of $Al_{0.6}In_{0.4}As$ as a top spacer, upper APD of Si, 200 Å of $Al_{0.6}In_{0.4}As$ as a Schottky barrier and 100 Å of $In_{0.53}Ga_{0.47}As$ as a cap doped at $5 \times 10^{18}\,cm^{-3}$. Five different wafers with different doping and channel grading schemes were grown as described in Table I. For wafer 8646, the channel was decreased from the 200 Å to 120 Å and for wafers 8649 and 8650 the channels were parbolically graded from 53 % to 71 % back to 53 % with the average at 65 %.

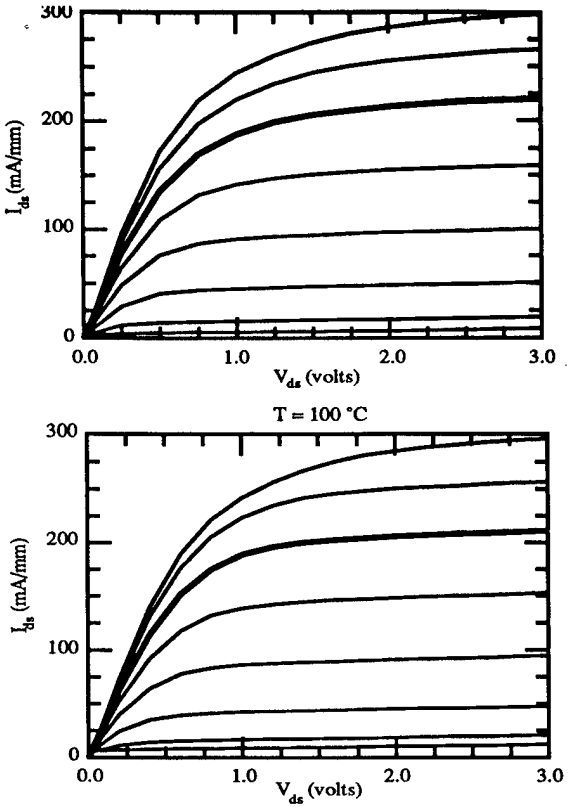
Table I Summary of the five double modulation doped wafers

wafer	channel	APD density (10^{12} cm^{-2})		% Indium		Graded
#	(Å)	upper	lower	X	Y	
8646	120	5	2	53	52	N
8647	200	5	2	53	52	N
8648	200	5.5	2.5	65	40	N
8649	200	6	3	65	40	Y
8650	200	6.5	3.5	65	40	Y

The devices were fabricated using two optical steps and one E-beam lithography step for the gates. The devices were mesa isolated by using a phosphoric acid:peroxide wet etch. A sidewall channel etch was performed with a selective citric acid:peroxide solution to eliminate the gate to InGaAs mesa contact (10). Ohmic contacts and e-beam alignment marks were defined with a second optical lithography step. The ohmic contacts were formed using Ni/AuGe/Ag/Au

which was alloyed at 340°C in an RTA for 10 sec producing contact resistances less than 0.1 Ω-mm. T-gates were then defined with an electron-beam and the gate recess was performed with a selective citric acid:peroxide wet etch.

Typical current-voltage characteristics at 25 °C and 100 °C for a 2 μm gate length 3D-SMODFET on wafer 8648 is shown in Fig(s). 6a and 6b, with limited degradation at 100 °C. The forward gate current at different temperatures is shown in Fig. 7a, with an effective barrier height > 1 eV extracted from an activation energy measurement (Fig. 7b). The low current (< 400 mA/mm) in the device is due to surface depletion in the linear regions around the gate between the source and drain ohmic contacts.



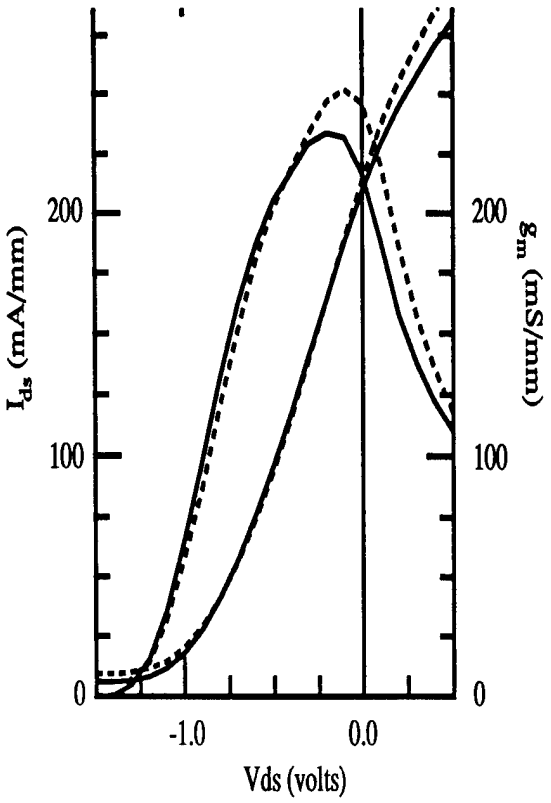


Figure 6b 2 μm x 100 μm (L_g x W_g) I_{ds}, g_m versus V_{gs} characteristics for a 3D-SMODFET at 25 °C (solid) and 100 °C dashed) [Vds = 2.0 V].

Figure 6a 2 μm x 100 μm (L_g x W_g) I_{ds} versus V_{ds} characteristics for a 3D-SMODFET at 25 °C and 100 °C [V_{gs} = +0.5 (top) to -1.25 (bottom) in 0.25 V steps].

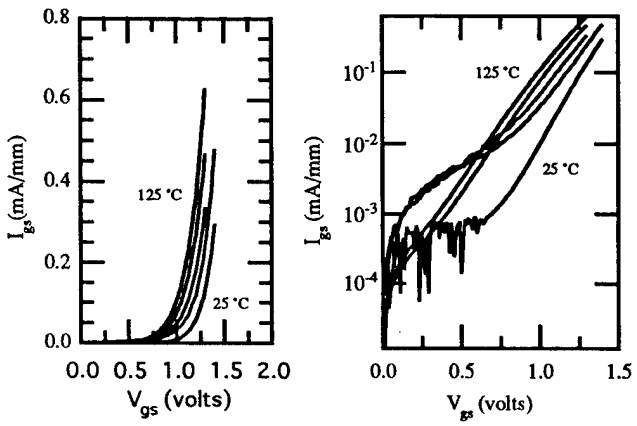


Figure 7a Forward gate current of a $Al_{0.6}In_{0.4}As$/ $In_{0.65}Ga_{0.35}As$/ $Al_{0.6}In_{0.4}As$ 3D-SMODFET on InP (2 μm x 100 μm) at 25 °C, 50 °C, 75 °C, 100 °C and 125 °C.

A change in the processing sequence has resulted in drain currents > 1000 mA/mm and a DC transconductance of > 500 mS/mm for wafer 8648 as shown in Fig(s). 8a and 8b. The devices have good pinch-off characteristics (< 2.5 V), output conductance (< 15 mS/mm), gate-drain breakdown (2.5 to 7 V) and good microwave performance with a high f_{MAX} to f_T ratio (330/110) for a 0.18 μm gate length. A summary of open channel current and hall data is shown in Table II.

Table II Summary of electrical results

Run #	V_t v	I_{oc} mA/mm	hall (300K)		hall (77 K)	
			μ (cm^2/Vsec)	n_s (10^{12} c m^{-2})	μ (cm^2/Vsec)	n_s (10^{12} c m^{-2})
8646	1.7	1100	6000	5.8	10,300	5.6
8647	1.6	1000	6900	5.7	12,100	5.4
8648	1.74	1200	7200	6.5	12,100	6.0
8649	2.1	1500	6700	7.7	11,800	7.2
8650	2.4	1850	6500	8.4	12,100	8.1

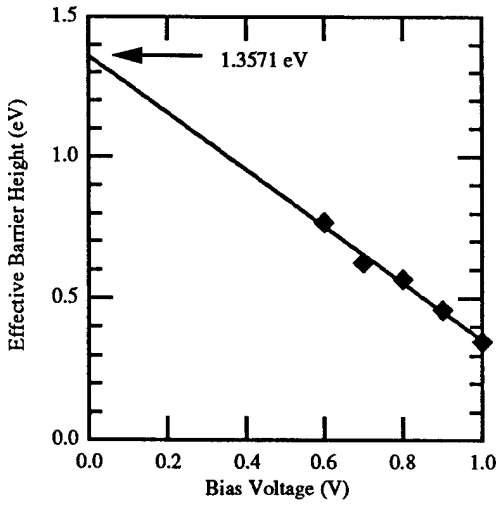


Figure 7b Effective barrier height (eV) for $Al_{.6}In_{.4}As/In_{.65}Ga_{.35}As/Al_{.6}In_{.4}As$ 3D-SMODFET on InP.

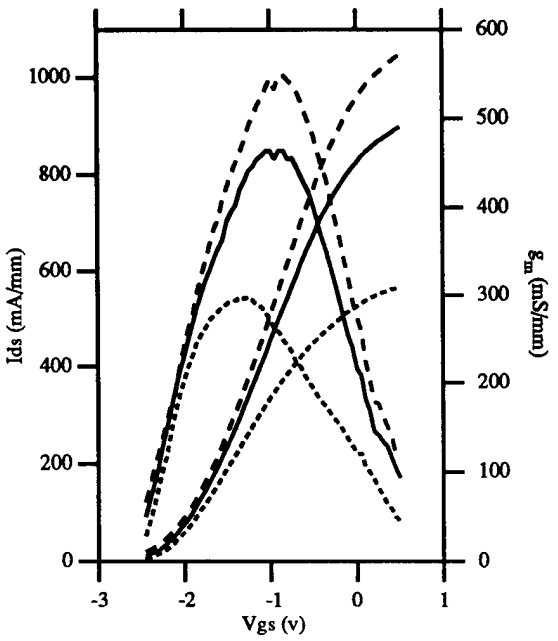


Figure 8a Current voltage (I_{ds} vs V_{gs}) characteristics of an $Al_{0.6}In_{0.4}As$/ $In_{0.65}Ga_{0.35}As$/$Al_{0.6}In_{0.4}As$ 3D-SMODFET on InP with a parabolically graded channel [V_{ds} = 0.5 V (dots), 1.0 V (solid), 1.5 V (dashed)].

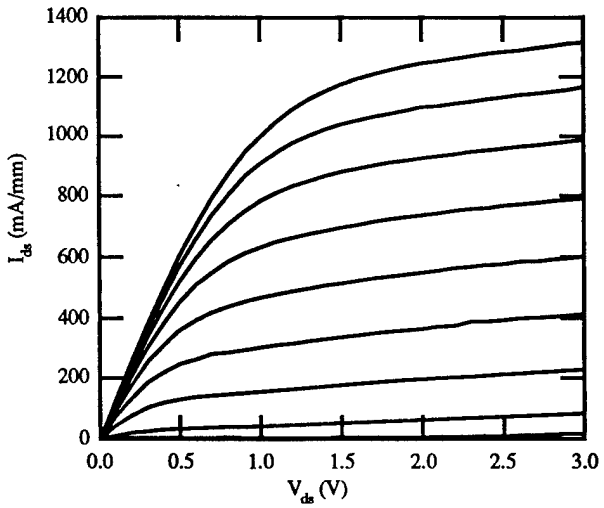


Figure 8b Current voltage (I_{ds} vs V_{ds}) characteristics of an $Al_{0.6}In_{0.4}As$/ $In_{0.65}Ga_{0.35}As$/$Al_{0.6}In_{0.4}As$ 3D-SMODFET on InP with a parabolically graded channel [V_{gs} = 0.0 (top), to -2.0 (bottom), 0.25 V steps].

2C. List of all publications and technical reports

"High Temperature Operation of AlInAs/InGaAs/AlInAs 3D-SMODFETs with Record Two Dimensional Electron Gas Densities," Glenn H. Martin, Allen Lepore, Matthew Seaford, Boris Pereiaslavets, Robert Spencer, Lester F.Eastamn, accepted for publication at the 1996 IEEE International Electron Devices Meeting, San Francisco, Dec. 1996

"Optimization of Narrow Channel 3D-SMODFETs," Glenn H. Martin, Matthew L. Seaford, Boris Pereiaslavets, J. Burm, Robert Spencer, Lester F.Eastamn, Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD), Santa Fe, New Mexico, Febuary 19-21, 1996

"Channel Width Optimization of 3D-SMODFETs on GaAs and InP," Glenn Martin, Matthew Seaford, Robert Spencer, Lester Eastman, Cornell Nanofabrication Facility (CNF) Affiliates Meeting, Cornell University, Oct. 1995

"Optimization of Graded Channel AlInAs/InGaAs 3D-SMODFETs on InP Substrates," Glenn H. Martin, Matthew L. Seaford, Robert Spencer, Lester F.Eastamn, Scott Massie and Dave Hartzell, 1995 NATO-ASI meeting in Sozopol, Bulgaria, Sept 20-29, 1995

"Optimization of 3D-SMODFETs on GaAs and InP substrates with a Simple Analytical Model," Glenn H. Martin, Matt Seaford, Robert Spencer, Jurgen Branstein, Lester Eastman, 15th Biennial IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Aug 7-9, 1995

"Computer Analysis of MODFET Structures on Indium Phosphide Substrates with Pseudomorphic Channels and Barriers with P-Layers", Glenn Martin, Matthew Seaford, Allen Lepore, Lester Eastman, Presented at Advanced Heterostructure Transistor Workshop, Hawaii, Dec 1994

"Narrow Channel GaInP/InGaAs/GaAs MODFET grown by MBE with record 2-DEG density for high frequency and power applications," Boris Pereiaslavets, Juergen Branstein, Glenn Martin, Lester Eastman, Bob Yanka, James Ballingall, Device Research Conference, Santa Barbara, Ca., June 1996

"Design of Narrow Channel GaInP/InGaAs/GaAs MODFET for High Frequency and Power Applications," Boris Pereiaslavets, Glenn Martin, Lester Eastman, accepted for presentation to the Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE), Vilnius, Lithuania,May 1996

"Subnanometer Analysis and Modeling of MBE grown InP BAsed

MODFETs" Matthew Seaford, Scott Massie, Dave Hartzell, Glenn Martin,Warren Wu, John Tucker, Lester F.Eastamn, Presented as a late paper at the 1996 Eighth International Conference on Indium Phosphide and Related Materials, Schwabish-Gmund, Germany, April 21-25 Accepted for publication to the Journal of Electronic Materials

"Optimization of the Spacer Layer Thickness in AlInAs/InGaAs/InP MODFETs," Matthew Seaford, Glenn Martin, Lester Eastman, Scott Massie, Dave Hartzell, accepted for publication in the Journal of Electronic Materials

"Improving the Schottky Barrier and Leakage Current of MODFETs grown on InP," Matthew Seaford, Glenn Martin, Scott Massie, Dave Hartzell, and Lester Eastman, Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE), Stockholm, Sweden, May 21-24, 1995

"Structure and Growth Optimization of Pseudomorphic MODFETs on InP", Matthew Seaford, Glenn Martin, Lester Eastman, Scott Massie, Dave Hartzell, MRS meeting in San Francisco, April, 1995

"Pursuit of Phonon Scattering Suppresiion in Short Period AlAs/GaAs Multiple Quantum Well Structures," T. LeTran, W. Schaff, B. Ridley, Y. Chen, A. Clark, L. Eastman, APL, march 1994

"On the Suppression of Phonon-Electron Scattering in Short Periodic AlAs/GaAs Multiple Quantum Well Structures," T. LeTran, W. Schaff, B. Ridley, Y. Chen, A. Clark, S. O'Keefe, L. Eastman, 4th Biennial IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, 11-21, Aug 2-4, 1993

2D List of all participating scientific personnel showing any advanced degrees earned by them while employed on the project

Jinwook Burm	PhD, May 1995
Alan Acker	MS, Jan 1996
Robert Spencer	PhD, Jan. 1997
Glenn H Martin	PhD, Expected 1997
Boris Pereiaslavets	PhD, Expected 1997
Matthew Seaford	PhD, Expected 1997
Trung LeTran	PhD, Expected 1997
Lester Eastman	
Bill Schaff	

3. Report of inventions

None

4. Bibliography

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2 M. Foisy, "A Physical Model for the Bias Dependence of the Modulation-Doped Field Effect Transistor's High-Frequency Performance," Ph.D. Dissertation, School of Electrical Engineering, Cornell University, 1990

3 H. Park, "Epitaxial Layer Design of Psuedomorphic MODFETs for High-Frequency Power Application," Ph.D. Dissertation, School of Electrical Engineering, Cornell University, 1992

4 D. Teng, P. Mandeville, L. Eastman, "Growth Limitations of Strained Multiple Quantum Wells," Journal Crystal Growth , July 1992

5 Glenn H. Martin, Matt Seaford, Robert Spencer, Jurgen Branstein, Lester Eastman, "Optimization of 3D-SMODFETs on GaAs and InP substrates with a Simple Analytical Model," 15th Biennial IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Aug 7-9, 1995

6 Matthew Seaford, Glenn Martin, L.F. Eastman, Dave Hartzell, Scott Massie, "Optimization of the Spacer Layer Thickness in AlInAs/InGaAs/InP MODFETs," Journal of Electronic Materials, Vol. 25, No. 9, 1551, 1996

7 Matthew Seaford, Scott Massie, Dave Hartzell, Glenn Martin, Warren Wu, John Tucker, Lester Eastman, "Subnaometer Analysis and Modeling of MBE grown InP based MODFETs," Journal of Elecronic Materials, Jan. 1997

8 Glenn Martin, Allen Lepore, Matt Seaford, Boris Pereiaslavets, Robert Spencer, Lester Eastman, "High Temperature Operation of AlInAs/InGaAs/AlInAs 3D-SMODFETs with Record Two-Dimensional Electron Gas Densities," International Electron Devices Meeting, San Francisco, Dec. 9, 1996